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L2	21	((FIFO adj (queue or memory)) same (instrumentation or statistic\$1)) and @ad<"20011211"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/04/03 15:11
L3	229	((FIFO) same (instrumentation or statistic\$1)) and @ad<"20011211"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/04/03 16:05
L4	8	((tri-state) same (instrumentation or statistic\$1)) and @ad<"20011211"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2006/04/03 16:06
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IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

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Cancelo, G.I.E.; Zimmermann, S.;
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[IEEE Std 1003.0-1995](#)
29 Dec. 1995
[AbstractPlus](#) | Full Text: [PDF](#)(1724 KB) IEEE STD
- ☐ 3. **Hardware/software codesign and rapid prototyping of embedded systems**
Slomka, F.; Dorfel, M.; Munzenberger, R.; Hofmann, R.;
[Design & Test of Computers, IEEE](#)
Volume 17, Issue 2, April-June 2000 Page(s):28 - 38
Digital Object Identifier 10.1109/54.844331
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(140 KB) IEEE JNL
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- ☐ 4. **Using VHDL for high-level, mixed-mode system simulation**
Srivastava, M.B.; Brodersen, R.W.;
[Design & Test of Computers, IEEE](#)
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Digital Object Identifier 10.1109/54.156156
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- ☐ **1. A 2.5 Gb/s ATM switch chip set**
Plaza, P.; Merayo, L.A.; Diaz, J.C.; Conesa, J.L.;
[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)
Volume 4, Issue 3, Sept. 1996 Page(s):405 - 416
Digital Object Identifier 10.1109/92.532040
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- ☐ **2. On the way to the 2.5 Gbits/s ATM network ATM multiplexer demultiplexer ASIC**
Riesco, J.; Diaz, J.C.; Merayo, L.A.; Conesa, J.L.; Santos, C.; Juarez, E.;
[European Design and Test Conference, 1997. ED&TC 97. Proceedings](#)
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- ☐ **3. Modeling and simulation of a readout architecture for pixel detectors**
Cancelo, G.I.E.; Zimmermann, S.;
[Nuclear Science, IEEE Transactions on](#)
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- ☐ **4. ATM traffic shaper: ATS**
Diaz, J.C.; Plaza, P.; Crespo, J.;
[Design, Automation and Test in Europe, 1998., Proceedings](#)
23-26 Feb. 1998 Page(s):96 - 101
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- ☐ **5. Warren: a low-cost ATM home area network**
Greaves, D.J.; Bradbury, R.J.;
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- ☐ 1. **A 2.5 Gb/s ATM switch chip set**
Plaza, P.; Merayo, L.A.; Diaz, J.C.; Conesa, J.L.;
[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)
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- ☐ 2. **Energy-effective issue logic**
Folegnani, D.; Gonzalez, A.;
[Computer Architecture, 2001. Proceedings. 28th Annual International Symposium on](#)
30 June-4 July 2001 Page(s):230 - 239
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[AbstractPlus](#) | [Full Text: PDF\(192 KB\)](#) IEEE CNF
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- ☐ 3. **On the way to the 2.5 Gbits/s ATM network ATM multiplexer demultiplexer ASIC**
Riesco, J.; Diaz, J.C.; Merayo, L.A.; Conesa, J.L.; Santos, C.; Juarez, E.;
[European Design and Test Conference, 1997. ED&TC 97. Proceedings](#)
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- ☐ 4. **ATM traffic shaper: ATS**
Diaz, J.C.; Plaza, P.; Crespo, J.;
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Le Pocher, H.; Leung, V.C.M.; Gillies, D.W.;
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- ☐ 2. **An ATM scheduler supporting all adaptation alternatives for real-time services**
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[Global Telecommunications Conference, 1998. GLOBECOM 98. The Bridge to Global](#)
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Christiansen, M.; Jeffay, K.; Ott, D.; Smith, F.D.;
[Networking, IEEE/ACM Transactions on](#)
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- ☐ 5. **Modeling and simulation of a readout architecture for pixel detectors**
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- ☐ 6. **Modeling and simulation of a readout architecture for pixel detectors**
Cancelo, G.I.E.; Zimmermann, S.;

- ☐ **7. Different queuing policies for handover requests in low Earth orbit mobile satellite systems**
Del Re, E.; Fantacci, R.; Giambene, G.;
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Volume 48, Issue 2, March 1999 Page(s):448 - 458
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- ☐ **8. Multipoint Private Line (MPL) Access Delay Under Several Interstation Disciplines**
Pack, C.; Whitaker, B.;
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- ☐ **9. Parallel image processing with the block data parallel architecture**
Alexander, W.E.; Reeves, D.S.; Gloster, C.S., Jr.;
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- ☐ **10. Performance evaluation of input and output queueing techniques in ATM switching systems**
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Golestani, S.J.; Bhattacharyya, S.;
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- ☐ **12. An approximation for performance evaluation of stationary single server queues**
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- ☐ **13. Maisie: a language for the design of efficient discrete-event simulations**
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- ☐ **14. Parameter estimation for partially observed queues**
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- ☐ **15. Performance Evaluation of a Variable Frame Multiplexer for Integrated Switched Networks**
Maglaris, B.; Schwartz, M.;
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- ☐ **16. Performance evaluation of client-server systems**
Ibe, O.C.; Choi, H.; Trivedi, K.S.;
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Volume 4, Issue 11, Nov. 1993 Page(s):1217 - 1229
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- ☐ **17. Handoff ordering using signal prediction priority queuing in personal communication systems**
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- ☐ **18. Bandwidth Allocation Strategies in Wide-Band Integrated Networks**
Kraimeche, B.; Schwartz, M.;
[Selected Areas in Communications, IEEE Journal on](#)
Volume 4, Issue 6, Sep 1986 Page(s):869 - 878
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- ☐ **19. Performance evaluation of adaptation functions in the ATM environment**
Stassinopoulos, G.I.; Venieris, I.S.; Petropoulos, K.P.; Protonotarios, E.N.;
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Volume 42, Issue 6, June 1994 Page(s):2335 - 2344
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- ☐ **20. A performance model for ATM switches with general packet length distributions**
Xi-Ren Cao; Towsley, D.;
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- ☐ **21. Multicast scheduling for input-queued switches**
Prabhakar, B.; McKeown, N.; Ahuja, R.;
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- ☐ **22. A passive test and measurement system: traffic sampling for QoS evaluation**
Cozzani, I.; Giordano, S.;
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23. Unsynchronized parallel discrete event simulation

Rao, D.M.; Thondugulam, N.V.; Radhakrishnan, R.; Wilsey, P.A.;

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24. Design Tradeoffs for Local Access Systems in Computer Networks

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25. Performance models of statistical multiplexing in packet video communications

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 Mehraban, B.; Kovalsky, L.;
[Power Engineering Society 1999 Winter Meeting, IEEE](#)
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 Tao Chen; Hong Ren Wu;
[Image Processing, IEEE Transactions on](#)
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- ☐ 3. **Adaptive impulse detection using center-weighted median filters**
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- ☐ 4. **Embedded hardware and software self-testing methodologies for processor cores**
 Li Chen; Dey, S.; Sanchez, P.; Sekar, K.; Ying Chen;
[Design Automation Conference, 2000. Proceedings 2000. 37th](#)
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- ☐ 5. **Structural analysis and generation of synthetic digital circuits with memory**
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[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)
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- ☐ **8. Subject index**
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Volume 8, Issue 12, Dec. 1999 Page(s):6 - 23
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- ☐ **10. Statistically determined static thermal ratings of overhead high voltage transmission lines in the Rocky Mountain region**
McElvain, F.R.; Mulnix, S.S.;
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- ☐ **11. Algorithms for max and min filters with improved worst-case performance**
Brookes, M.;
[Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on \[see also](#)
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- ☐ **12. A CMOS buffer without short-circuit power consumption**
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- ☐ **13. Image denoising: a nonlinear robust statistical approach**
Ben Hamza, A.; Krim, H.;
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Chandrakasan, A.P.; Potkonjak, M.; Mehra, R.; Rabaey, J.; Brodersen, R.W.;
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)

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- ☐ **15. Low-power encodings for global communication in CMOS VLSI**
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